IV. REMARKS

Claims 23-32 are pending and stand rejected. Claims 23 and 28 have been amended. Attached hereto is Appendix A showing the changes made to the amended claims. Reconsideration is respectfully requested.

1. Objection to Drawings

Figures 1A-1C were objected to for not including a legend such as --Prior Art--. Submitted herewith are amended Figs. 1A-1C with --(Prior Art)-- legends added in red. Approval of the amended figures is respectfully requested. A separate letter to the Official Draftsperson is also submitted herewith.

2. Objection to Title

The title was objected to for not being descriptive. The title has been amended to reflect the restriction requirement in this case and that the method claims have been cancelled.

Approval of the title is respectfully requested.

3. Rejection of Claims 23 and 24 Under § 103(a)

Claims 23-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,811,853 (Wang), U.S. Patent No. 5,493,138 (Koh) and U.S. Patent 6,091,104 (Chen '104). The applicant respectfully traverses this rejection.

It is impermissible simply to engage in a hindsight reconstruction of the claimed invention using the applicant's structure as a template and selecting elements from references to fill the gaps. Interconnect Planning, 774 F.2d at 1143, 227 USPQ at 551. The references themselves must provide some teaching whereby the applicant's combination would have been obvious. Id. It is respectfully submitted that the Examiner is merely combining features from different references to yield the claimed invention, without sufficient teaching or motivation for the combination. For example, claim 23 recites the combination of the first and second insulation layers, the floating gate, the control gate, and the alignment between the control gate vertical sidewall portion and the second region. The Examiner admits that the combination of

Wang and Koh fails to teach this combination. However, on pages 3-4 of the Office Action, the Examiner states it would have been obvious to modify the Wang device by aligning the edge of the impurity region with the edge of the gate vertical sidewall and a spacer as taught by Chen '104 "to improve the performance of the device". The Examiner cites Column 3, lines 38-40 of Chen '104 as the source of motivation for such a combination. However, the cited text is merely a general object of the disclosed invention as a whole, with no explicit or implicit reference to the claimed alignment between the gate vertical sidewall and the impurity region, or how that feature would add benefit to other structures. The Applicant respectfully submits that there is no teaching, suggestion or incentive supporting the combination of Wang, Koh and Chen '104.

Notwithstanding the above, claim 23 has been amended to further recite that the second insulation layer has a first portion disposed over the first insulation layer and the substrate, a second portion disposed adjacent the floating gate and a third portion disposed over the floating gate, where the control gate first portion is disposed over the first insulation layer first portion and adjacent to the first insulation layer second portion, and the control gate second portion extends over the second insulation layer third portion. The cited references fail to teach or suggest the combination of recited elements. Specifically, none of the references teach the second insulation layer (for Fowler-Nordheim tunneling) extending, inter alia, under the control gate and over the first insulation layer and substrate, as well as adjacent and over the floating gate, as recited by claim 23.

It is therefore submitted that claim 23 (as amended), and claim 24 dependent thereon, are not rendered obvious by Wang, Koh, and Chen '104.

4. Rejection of Claims 25 and 26 Under § 103(a)

Claims 25-26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of admitted Prior Art Figure 1C. Claims 25-26 depend from claim 23, and are therefore considered allowable for the reasons set forth in Part 3 above.

5. Rejection of Claim 27 Under § 103(a)

Claim 27 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 5,751,048 (Lee). Claim 27 depends from claim 23, and is therefore considered allowable for the reasons set forth in Part 3 above.

6. Rejection of Claims 28 and 29 Under § 103(a)

Claims 28-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, and in further view of U.S. Patent No. 6,140,182 (Chen '182).

Claim 28 has been amended in the same manner as claim 23, to specify the first, second and third portions of the second insulation layer, and to specify the first and second control gate portions in relation to the three second insulation layer portions. The addition of Chen '182 does not appear to overcome the shortcomings of Wang, Koh, and Chen '104. Therefore, for the reasons set forth in Part 3 above, it is submitted that claim 28 as amended, along with claim 29 dependent thereon, are not rendered obvious by these references.

7. Rejection of Claims 30 and 31 Under § 103(a)

Claims 31-32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of admitted Prior Art Figure 1C. Claims 30-31 depend from claim 28, and are therefore considered allowable for the reasons set forth in Part 6 above.

8. Rejection of Claim 32 Under § 103(a)

Claim 32 was rejected under 35 U.S.C. 103(a) as being unpatentable over Wang, Koh, Chen '104, Chen '182, and in further view of Lee. Claim 32 depends from claim 28, and is therefore considered allowable for the reasons set forth in Part 6 above.

For the foregoing reasons, it is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

Respectfully submitted,

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APPENDIX A: MARKINGS TO SHOW CHANGES MADE

23. (Amended) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region;

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed [and] adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has [and having] a thickness permitting Fowler-Nordheim tunneling of charges therethrough;

an electrically conductive control gate having a first portion disposed over the first insulation layer first portion and adjacent to the first insulation layer second portion, [and insulated from the floating gate] and a second portion extending over [a portion of] the second insulation layer [and a] third portion [of the floating gate], the control gate having a substantially vertical sidewall portion; and

an insulation spacer formed adjacent to the substantially vertical sidewall portion of the control gate;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.

28. (Amended) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of the channel region and over a portion of the first region, and

a second insulation layer having a first portion disposed over said first insulation layer and said substrate, a second portion disposed [and] adjacent the floating gate and a third portion disposed over the floating gate, wherein the second insulation layer has [having] a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion and a second portion, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the control gate first portion is positioned over the second insulation layer first portion and adjacent to the second insulation layer second portion and [the floating gate and] the control gate second portion [partially] extends over the second insulation layer third portion [and the floating gate], and wherein each of the control gates has a substantially vertical sidewall portion; and

a plurality of insulation spacers each formed adjacent to one of the substantially vertical sidewall portions of the control gates;

wherein the second region has an edge that is aligned with the substantially vertical sidewall portion.